

SDS

SCIENTIFIC DATA SYSTEMS



SDS 9300 Computer

SDS 9300 The SDS 9300 is a general-purpose digital computer comparable in speed and other features with large-scale scientific and systems computers. In price, however, the 9300 is comparable to medium-scale computers — basic *system* prices start at approximately \$250,000. The 9300 thus represents a significant reduction in the cost-per-answer of computing equipment.

The SDS 9300 is the third computer manufactured by Scientific Data Systems. It is logically and electrically similar to the other SDS computers — the SDS 910 and the SDS 920 — and incorporates the same high degree of reliability and flexibility.

The SDS 9300 has the following characteristics:

- 24-bit word plus a parity bit
- 48-bit word for floating point arithmetic
- 3 Index Registers and Indirect Addressing
- Basic memory of 4096 words expandable to 32,768 words, all directly addressable, with:
 - 0.7 μ sec access time
 - 1.75 μ sec cycle time
- Memory non-volatile with power failure
- Execution times, including all accesses *and indexing* (using overlapped memories):

Fixed Point

1.75 μ sec	Add
3.5 μ sec	Double Precision Add
7.0 μ sec	Multiply
5.25 μ sec	Shift (24 positions)

Floating Point

(39-bit mantissa, 9-bit exponent)

14.0 μ sec	Add
12.25 μ sec	Multiply

- Extensive repertoire of powerful instructions (more than 110)
- Byte operations which permit manipulation of 3, 6, 9, 12, 15, 18, or 21-bit Bytes. Two 12-bit Bytes may be multiplied in 3.5 microseconds
- 6-bit Flag Register with set/reset/test instructions which provides fast, easy-to-use program switches for logical decision making. Each position may be set or reset under program control and the status used to control program flow
- 11 high-speed search operations operate at 1.75 microseconds per item
- Multi-level indexing and indirect addressing

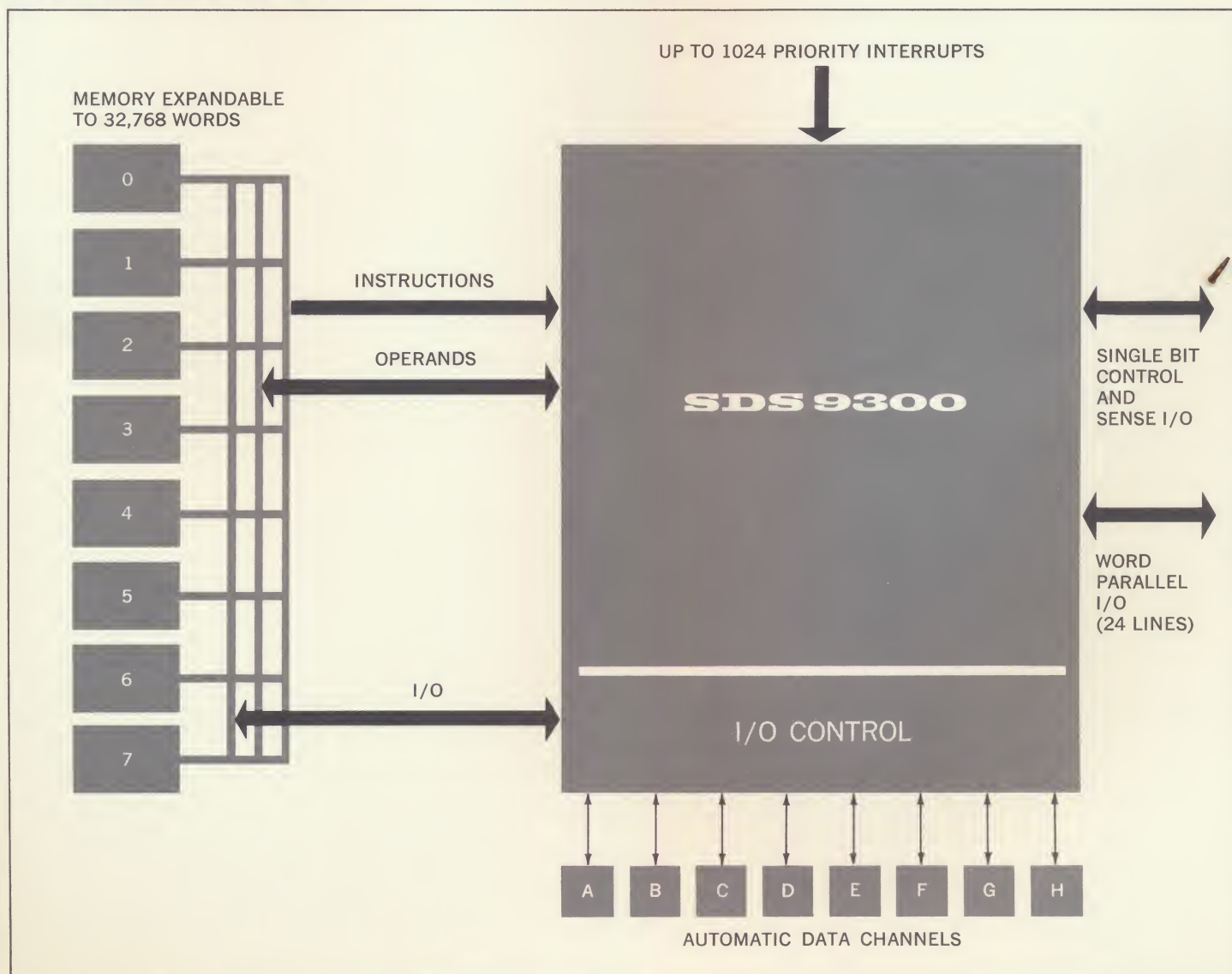
- Index Registers which contain and operate with a base value and an increment or decrement
- REPEAT instruction which operates with variable size incrementing or decrementing; when used with Input/Output, permits Gather-Read and Scatter-Write
- Extensive shift and inter-register instructions for data manipulation
- Flexible and easily programmed subroutine execution
- Up to 8 Automatic Data Channels each capable of fully buffered operation at one word every 1.75 microseconds *simultaneously* with full speed computation
- Automatic Data Channels which operate upon either words or characters. The number of characters per word is under program control
- Addressing of I/O operations can be both indexed and indirect to facilitate Gather and Scatter operations
- Parity checking of Memory and I/O operations
- Searching of magnetic tape, discs, etc., can be accomplished independently of the memory and requires no computer time
- A Parallel Word I/O system in addition to the Automatic Data Channels to facilitate operation upon certain types of asynchronous information under program control
- SDS 910 available as a satellite I/O Processor
- Up to 32,000 output control signals and input test signals
- A complete priority interrupt system with up to 1024 priority levels. These can be individually enabled and disabled under program control
- Automatic program loading from cards, paper tape, magnetic tape, drums or discs
- Complete display of all programmable registers with extensive manual controls
- Six Sense Switches, two Manual Interrupt Switches and a Selective Halt provide complete capability for console control during execution
- FORTRAN, Symbolic Assembler, and a Monitor System as part of a complete software package
- No air conditioning required for computer proper — operating temperature range 10°C to 40°C
- Small size and simple installation — over-all dimensions, including expanded memory, approximately 6 x 8 x 2 feet plus an operator's console
- Low power requirements: 4 KVA
- All silicon semi-conductors for high reliability; small component count yields long Mean Time Between Failures

SDS 9300 ORGANIZATION The block diagram illustrates the organization of the SDS 9300. Up to 8 blocks of memory, each having 4096 words, can be employed. If the operand and instruction locations are in different blocks, the computer automatically overlaps accesses and thus eliminates one memory cycle time in the execution of the instruction. If an I/O operation employing an Automatic Data Channel is required, it can be carried on simultaneously with computation if the

affected address is in a block other than those used for operands and instructions. If the same block is indicated, one memory cycle is automatically taken from the main program.

In addition to the Automatic Data Channels, three other types of I/O are shown. The first consists of up to 1024 channels of priority interrupt. The second consists of up to 32,000 output Control lines and the same number of input Sense lines. The third is the word Parallel I/O under program control.

SDS 9300 BLOCK DIAGRAM



SDS 9300 INPUT/OUTPUT Four types of I/O are provided in the SDS 9300:

Automatic Data Channels Up to 8 Automatic Data Channels each provide transfer rates in excess of 550,000 words per second or in excess of 1,000,000 characters (IBM format) per second, simultaneous with and independent of computation. The Data Channel interrupts computation only if the I/O operation requires access to a Memory Block that is in use by the main program. In this case, 1.75 microseconds per word is required.

All Data Channels are bi-directional, operate on either words or characters and each can communicate with up to 64 I/O devices. In the case of character-oriented devices, assembly, disassembly, and parity manipulations are automatic. At the start of an I/O operation, the channel is loaded with the following information and proceeds independently of the computer proper:

a. Number of words to be processed (Count Control)
Up to 32,768

b. Address of first word
This address may be both indexed and indirect

c. Binary or BCD mode
Either IBM format can be used

d. Number of characters per word

e. Transmit or Non-Transmit

In Search, Erase and certain other operations, data need not be entered into or removed from memory

f. Interrupt Mode

Upon the completion of an I/O operation, or an end of file indication, or upon the detection of a parity error, the main program can, at the programmer's option, be interrupted

g. Channel Command

The following Channel Commands permit reading and writing of a complete or partial record, or a given number of words independent of inter-record gaps:

1. INPUT/OUTPUT OF A RECORD AND PROCEED
2. INPUT/OUTPUT OF A RECORD AND DISCONNECT
3. INPUT/OUTPUT UNDER COUNT CONTROL AND PROCEED
4. INPUT/OUTPUT UNDER COUNT CONTROL AND DISCONNECT
5. INPUT/OUTPUT UNTIL SIGNAL AND PROCEED
6. INPUT/OUTPUT UNTIL SIGNAL AND DISCONNECT
7. INPUT/OUTPUT UNDER COUNT CONTROL TO END OF RECORD AND PROCEED

8. INPUT/OUTPUT UNDER COUNT CONTROL TO END OF RECORD AND DISCONNECT

Word Parallel I/O Two instructions are provided in the SDS 9300 to permit the I/O of any word in memory under program control. The PARALLEL INPUT instruction, upon execution, places into the specified memory location the information on 24 input lines. The PARALLEL OUTPUT instruction outputs the word in the specified location to 24 lines. Note that this type of I/O is independent of the Automatic Data Channels and can operate *simultaneously* with them. If used with the REPEAT instruction, the Word Parallel I/O operates as an additional high-speed I/O channel.

Single Bit Control and Sense Two instructions provide for ON-OFF control signals. The first, EOM, generates one of 32,000 combinations of the 15 address bits of the instruction. By external decoders, these can be employed as control signals. The second instruction, SKS, is the inverse: it tests up to 32,000 lines and skips as a function of the result.

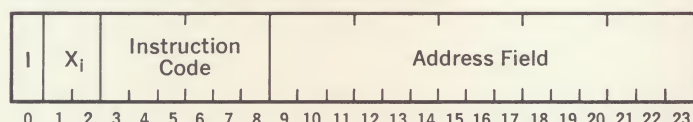
Priority Interrupt The SDS 9300 provides up to 1024 channels of Priority Interrupt. When an interrupt occurs, the program at the completion of the ongoing instruction, traps to the location assigned to that channel. All channels have an assigned priority and can be interrupted only by a channel of higher priority. The subroutine servicing instructions permit the program to service the interrupts in the correct order and to return to the main program after all interrupts have been serviced.

In certain cases, it is appropriate to deactivate one or a number of interrupt channels, effectively changing the priority configuration. An Arm-Disarm feature is provided for this function. The two highest priority channels are reserved for the Power Fail-Safe System. This system stores all volatile information in the event of a power failure and restores this information when the power is restored. These two interrupts cannot be disarmed.

SDS 9300 PERIPHERAL EQUIPMENT A wide variety of on/off-line peripheral equipment can be used with the SDS 9300. These include:

- Paper Tape I/O equipment
- High and low-speed Card Punches
- High and low-speed Card Readers
- High and low-speed Printers
- Multi-density high and low-speed Magnetic Tape Handlers
- Magnetic Drums
- Magnetic Discs

SDS 9300 INSTRUCTION FORMAT The instruction word format of the SDS 9300 is as follows:



Bit Number

0

Function

Indirect Address Bit—A “one” causes the computer to interpret bits 9-23 of the instruction (possibly modified by indexing) as the memory location where the effective address of the instruction may be found. A “zero” causes bits 9-23 (possibly modified by index-

1-2

3-8

9-23

ing) to be interpreted as the effective address of the instruction.

Index Register Bits—A non-zero entry in these positions causes the contents of bits 9-23 of the appropriate Index Register to be added to the address portion of the instruction prior to execution. Three Index Registers are provided, each of which contains both a base value and an increment.

Instruction Code—These 6 bits determine the operation to be performed.

Address—These bits normally determine the memory address referenced by the instruction code.

SDS 9300 INSTRUCTION LIST

Timing With Overlap (1 cycle = 1.75 μ sec)			Timing With Overlap (1 cycle = 1.75 μ sec)			Timing With Overlap (1 cycle = 1.75 μ sec)		
Instruction			Instruction			Instruction		
LOAD-STORE	Load A	1	REGISTER	Copy A into B, Clear A	1	SHIFT GROUP	Right Shift A	2-7
	Store A	2		Copy B into A, Clear B	1		Right Shift B	2-7
	Load B	1		Change	1		Right Shift Double	2-7
	Store B	2		GROUP	1		Right Shift A and B	2-7
	Load Index	1		(Contd.)	1		Logical Right Shift A	2-7
	Store Index	2		Merge A into B	1		Logical Right Shift Double	2-7
	Store Zero	2		Merge B into A	1		Logical Right Shift A and B	2-7
	Load Double Precision	2		Form Mask in B	1		Right Cycle A	2-7
	Store Double Precision	3		Form Mask in A	1		Right Cycle B	2-7
	Exchange M and A	2		Copy Index into A	1		Right Cycle Double	2-7
	Exchange M and B	2		Copy Index into B	1		Right Cycle A and B	2-7
	Load Selective	1		Copy A into Index	1		Left Shift A	2-5
	Store Selective	2		Copy B into Index	1		Left Shift B	2-5
	Exchange Memory and Index	2		Copy Index 1 into Index	1		Left Shift Double	2-5
				Copy Index 2 into Index	1		Left Shift A and B	2-5
ARITHMETIC GROUP	Add M to A	1	BRANCH GROUP	Copy Index 3 into Index	1		Logical Left Shift A	2-5
	Double Precision Add	2		Exchange Index and A	1		Logical Left Shift Double	2-5
	Subtract	1		Exchange Index and B	1		Logical Left Shift A and B	2-5
	Double Precision Subtract	2		Clear Index	1		Logical Left Shift Double	2-5
	Memory Plus One	2		Address to Index Base	1		Left Cycle A	2-5
	Memory Plus Two	2		Branch Unconditionally	1		Left Cycle B	2-5
	Multiply	4		Increase Index and Branch	1 or 2		Left Cycle Double	2-5
	Divide	9		Branch and Clear Interrupt	1		Left Cycle A and B	2-5
	Add A to M	2		Mark Place and Branch	2		Normalize A	2-5
	Twin Multiply	4		Branch and Mark Place of Argument Address	2		Normalize Double	2-5
FLOATING POINT GROUP	Double Precision Negate	1		Branch Return	2	CONTROL	Halt	1
	Floating Add	6-10	TESTS/SKIP	Skip if A Equals M	2 or 3		No Operation	1
	Floating Subtract	6-10		Skip if A Unequal to M	2 or 3		Execute	1
	Floating Multiply	7		Skip if A Greater than M	2 or 3		Copy Effective Address into Index Register 1	1
LOGICAL GROUP	Floating Divide	16		Skip if A Less than M	2 or 3		Repeat Instruction in M	2 + N(T)
	Extract	1		Reduce M, Skip if Negative	3	INPUT/OUTPUT	Energize Output M	1
	Merge	1		Skip if A = M on B Mask	2 or 3		Parallel Input	3
REGISTER CHANGE GROUP (Word or Byte)	Exclusive OR	1		Skip if M Negative	2 or 3		Parallel Output	2
	Copy Negative Into A	1		Skip if M and A Do Not Compare Ones	2 or 3		A Channel to Memory	3
	Clear A	1		Skip if M and B Do Compare Ones	2 or 3		Memory to A Channel	2
	Clear B	1		Skip if Bit Sum Even	2 or 3	FLAG REGISTER	Flag Indicators Reset/Set	1
	Clear AB	1		Skip if Signal Not Set	1 or 2		Flag Indicator Set Test/Reset	1 or 2
	Copy A into B	1		Skip if Floating Exponent in B $\geq$ M	2 or 3		Flag Indicator Reset Test/Set	1 or 2
	Copy Inverse of A into B	1		Skip if Masked Quantity in A Greater than M	2 or 3		Flag Indicator Reset/Set Test	1 or 2
	Copy B into A	1					Sense Switch Test	1 or 2
	Exchange A and B	1						
	Copy Inverse of B into A	1						

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